

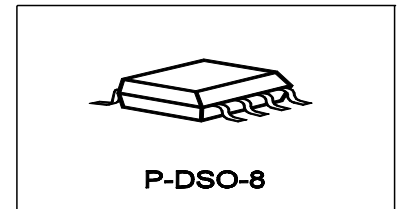
Smart Dual Lowside Power Switch

Features

- Logic Level Input
- Input Protection (ESD)
- Thermal shutdown with auto restart
- Overload protection
- Short circuit protection
- Overvoltage protection
- Current limitation
- Analog driving possible

Product Summary

Drain source voltage	V_{DS}	42	V
On-state resistance	$R_{DS(on)}$	200	m Ω
Nominal load current	$I_{D(Nom)}$	1.3	A
Clamping energy	E_{AS}	150	mJ

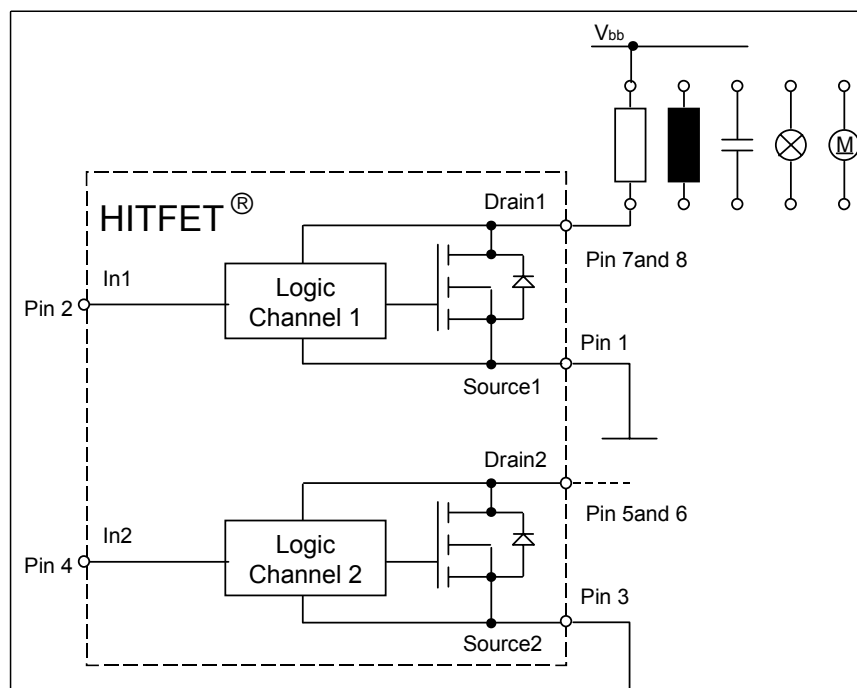


Application

- All kinds of resistive, inductive and capacitive loads in switching or linear applications
- μ C compatible power switch for 12 V DC applications
- Replaces electromechanical relays and discrete circuits

General Description

N channel vertical power FET in Smart SIPMOS® technology. Fully protected by embedded protection functions.

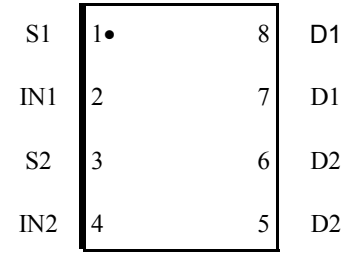


Complete product spectrum and additional information <http://www.infineon.com/hitfet>

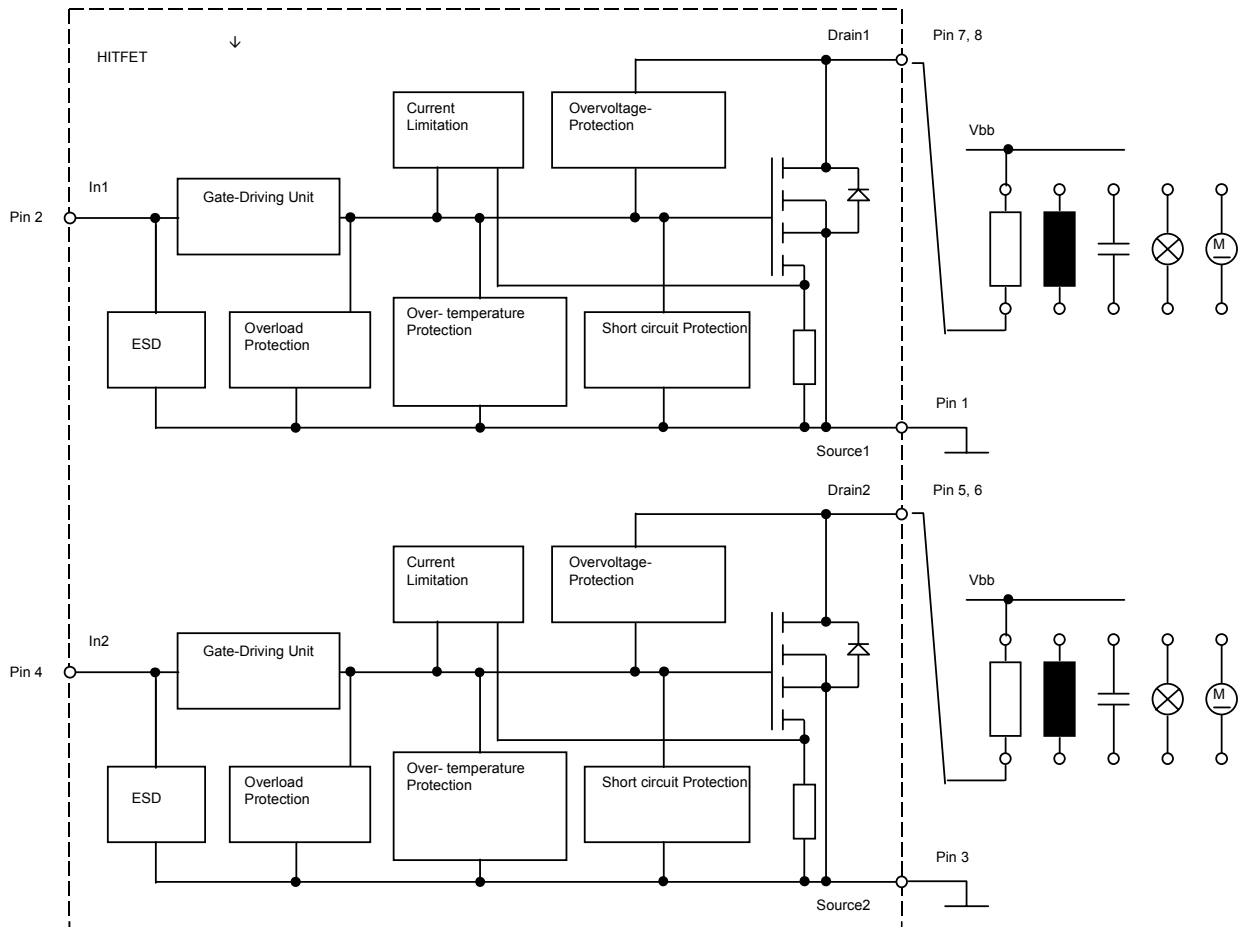
Pin Description

Pin	Symbol	Function
1	S1	Source Channel 1
2	IN1	Input Channel 1
3	S2	Source Channel 2
4	IN2	Input Channel 2
5	D2	Drain Channel 2
6	D2	Drain Channel 2
7	D1	Drain Channel 1
8	D1	Drain Channel 1

Pin Configuration (Top view)



P-DSO-8-7



Maximum Ratings at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	42	V
Drain source voltage for short circuit protection ¹⁾ $T_j = -40 \dots 150^\circ\text{C}$	$V_{DS(SC)}$	18	
Continuous input current ¹⁾ $-0.2\text{V} \leq V_{IN} \leq 10\text{V}$ $V_{IN} < -0.2\text{V}$ or $V_{IN} > 10\text{V}$	I_{IN}	no limit $ I_{IN} \leq 2$	mA
Operating temperature	T_j	$-40 \dots +150$	$^\circ\text{C}$
Storage temperature	T_{stg}	$-55 \dots +150$	
Power dissipation ²⁾⁵⁾ $T_A = 85^\circ\text{C}$	P_{tot}	0.8	W
Unclamped single pulse inductive energy ¹⁾ each channel	E_{AS}	150	mJ
Load dump protection $V_{LoadDump}^{1)3)} = V_A + V_S$ $V_{IN} = 0$ and 10V , $t_d = 400\text{ms}$, $R_I = 2\ \Omega$, $R_L = 9\ \Omega$, $V_A = 13.5\text{V}$	V_{LD}	50	V
Electrostatic discharge voltage¹⁾ (Human Body Model) according to Jedec norm EIA/JESD22-A114-B, Section 4	V_{ESD}	2	kV
Jedec humidity category, J-STD-20-B		MSL1	
IEC climatic category; DIN EN 60068-1		40/150/56	

Thermal resistance

junction - ambient: per channel @ 6cm^2 cooling area ²⁾	R_{thJA}		K/W
one channel on		100	
both channels on		160	

¹⁾ not subject to production test, specified by design

²⁾ Device on $50\text{mm} \times 50\text{mm} \times 1.5\text{mm}$ epoxy PCB FR4 with 6cm^2 (one layer, $70\mu\text{m}$ thick) copper area for drain connection. PCB mounted vertical without blown air.

³⁾ $V_{Loaddump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

⁵⁾ not subject to production test, calculated by R_{thJA} and $R_{ds(on)}$

Electrical Characteristics

Parameter at $T_j = 25^\circ\text{C}$, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Drain source clamp voltage $T_j = -40 \dots +150$, $I_D = 10 \text{ mA}$	$V_{DS(AZ)}$	42	-	55	V
Off-state drain current $T_j = -40 \dots +150^\circ\text{C}$ $V_{DS} = 32 \text{ V}$, $V_{IN} = 0 \text{ V}$	I_{DSS}	-	1.5	10	μA
Input threshold voltage $I_D = 0.3 \text{ mA}$, $T_j = 25^\circ\text{C}$ $I_D = 0.3 \text{ mA}$, $T_j = 150^\circ\text{C}$	$V_{IN(th)}$	1.3 0.8	1.7 -	2.2 -	V
On state input current	$I_{IN(on)}$	-	10	30	μA
On-state resistance $V_{IN} = 5 \text{ V}$, $I_D = 1.4 \text{ A}$, $T_j = 25^\circ\text{C}$ $V_{IN} = 5 \text{ V}$, $I_D = 1.4 \text{ A}$, $T_j = 150^\circ\text{C}$	$R_{DS(on)}$	- -	190 350	240 480	$\text{m}\Omega$
On-state resistance $V_{IN} = 10 \text{ V}$, $I_D = 1.4 \text{ A}$, $T_j = 25^\circ\text{C}$ $V_{IN} = 10 \text{ V}$, $I_D = 1.4 \text{ A}$, $T_j = 150^\circ\text{C}$	$R_{DS(on)}$	- -	150 280	200 400	
Nominal load current per channel ⁵⁾ $V_{DS} = 0.5 \text{ V}$, $T_j < 150^\circ\text{C}$, $V_{IN} = 10 \text{ V}$, $T_A = 85^\circ\text{C}$, one channel on both channels on	$I_{D(Nom)}$	1.3 1	1.65 1.3	- -	A
Current limit (active if $V_{DS} > 2.5 \text{ V}$) ²⁾ $V_{IN} = 10 \text{ V}$, $V_{DS} = 12 \text{ V}$, $t_m = 200 \mu\text{s}$	$I_{D(lim)}$	5	7.5	10	

¹not subject to production test, specified by design

²Device switched on into existing short circuit (see diagram Determination of $I_{D(lim)}$). If the device is in on condition and a short circuit occurs, these values might be exceeded for max. 50 μs .

⁵not subject to production test, calculated by R_{THJA} and $R_{DS(on)}$

Electrical Characteristics

Parameter at $T_j = 25^\circ\text{C}$, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	

Dynamic Characteristics

Turn-on time V_{IN} to 90% I_D : $R_L = 4.7 \Omega$, $V_{IN} = 0$ to 10 V, $V_{bb} = 12$ V	t_{on}	-	45	100	μs
Turn-off time V_{IN} to 10% I_D : $R_L = 4.7 \Omega$, $V_{IN} = 10$ to 0 V, $V_{bb} = 12$ V	t_{off}	-	60	100	
Slew rate on 70 to 50% V_{bb} : $R_L = 4.7 \Omega$, $V_{IN} = 0$ to 10 V, $V_{bb} = 12$ V	$-dV_{DS}/dt_{on}$	-	0.4	1.5	V/ μs
Slew rate off 50 to 70% V_{bb} : $R_L = 4.7 \Omega$, $V_{IN} = 10$ to 0 V, $V_{bb} = 12$ V	dV_{DS}/dt_{off}	-	0.6	1.5	

Protection Functions¹⁾

Thermal overload trip temperature	T_{jt}	150	175	-	$^\circ\text{C}$
Thermal hysteresis ²⁾	ΔT_{jt}	-	10	-	K
Input current protection mode	$I_{IN(Prot)}$	25	50	300	μA
Input current protection mode $T_j = 150^\circ\text{C}$	$I_{IN(Prot)}$	-	40	300	
Unclamped single pulse inductive energy ²⁾ each channel $I_D = 0.9$ A, $T_j = 25^\circ\text{C}$, $V_{bb} = 12$ V	E_{AS}	150	-	-	mJ

Inverse Diode

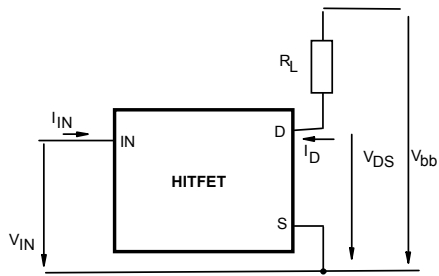
Inverse diode forward voltage $I_F = 7$ A, $t_m = 250 \mu\text{s}$, $V_{IN} = 0$ V, $t_P = 300 \mu\text{s}$	V_{SD}	-	1	-	V
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¹⁾ Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

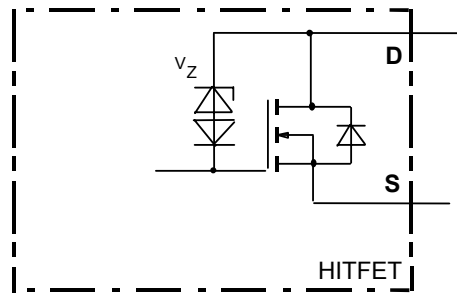
²⁾ not subject to production test, specified by design

Block diagram

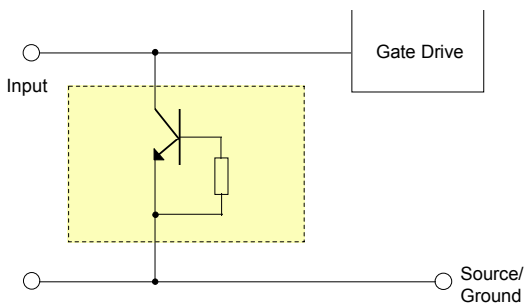
Terms



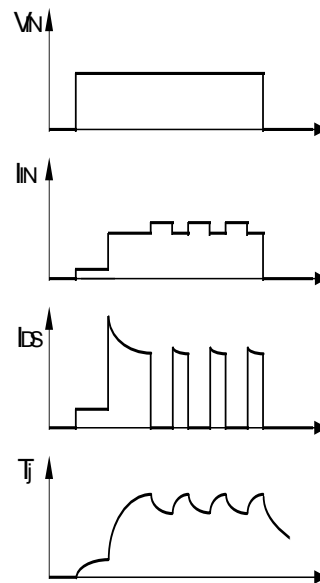
Inductive and overvoltage output clamp



Input circuit (ESD protection)

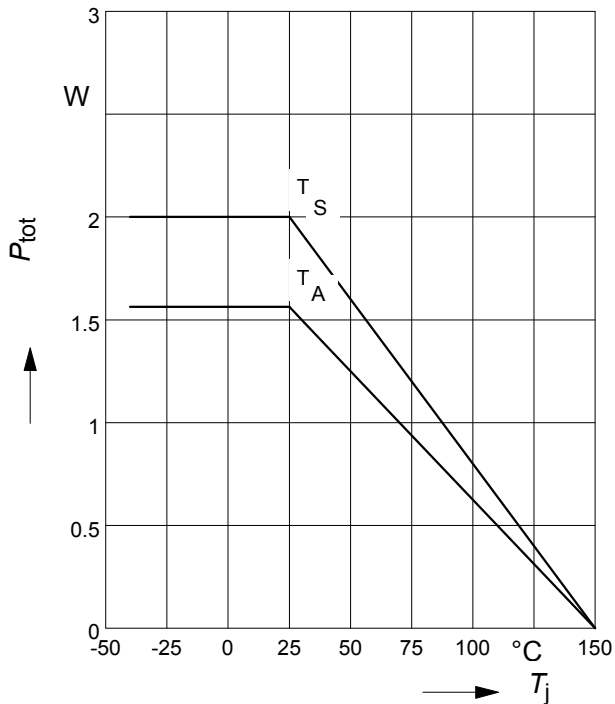


Short circuit behaviour



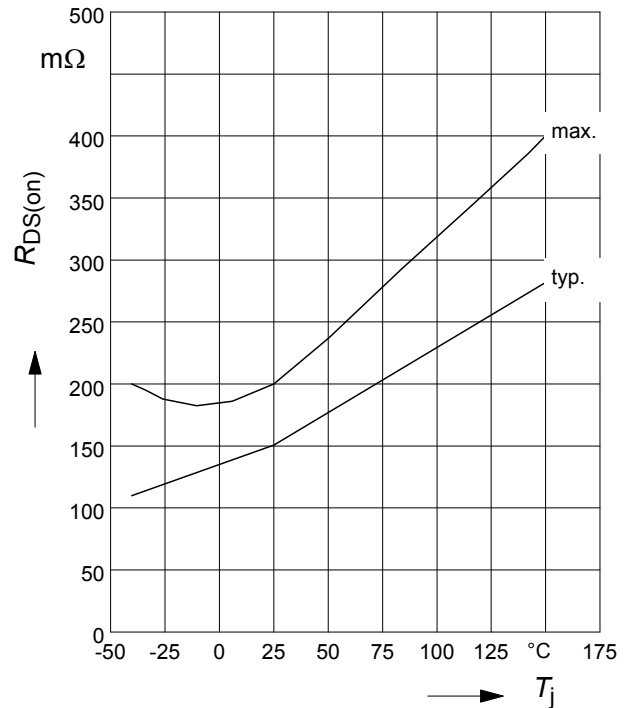
1 Overall maximum allowable power dissipation; $P_{tot} = f(T_S)$ resp.

$P_{tot} = f(T_A) @ R_{thJA} = 80 \text{ K/W}$



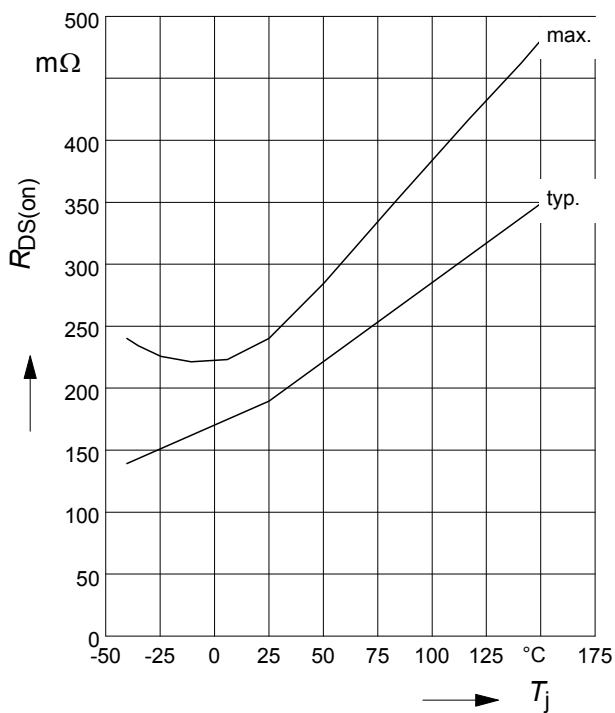
2 On-state resistance

$R_{ON} = f(T_j); I_D = 1.4A; V_{IN} = 10V$



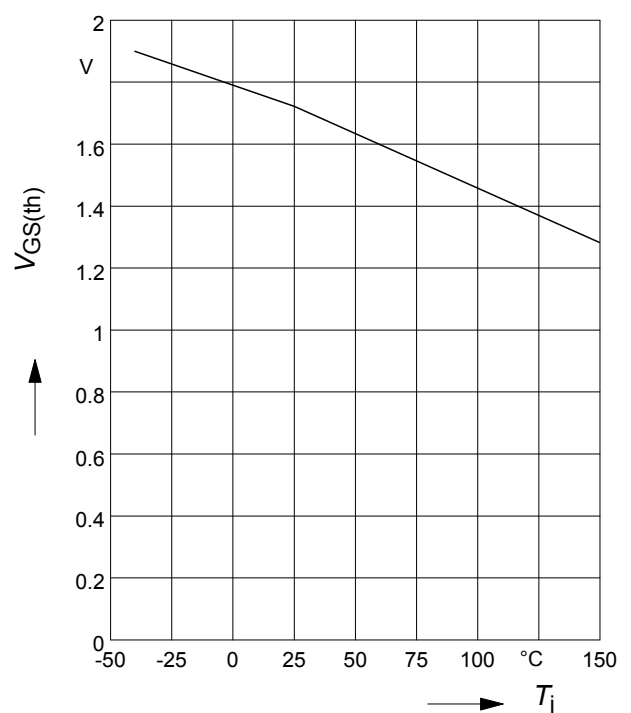
3 On-state resistance

$R_{ON} = f(T_j); I_D = 1.4A; V_{IN} = 5V$



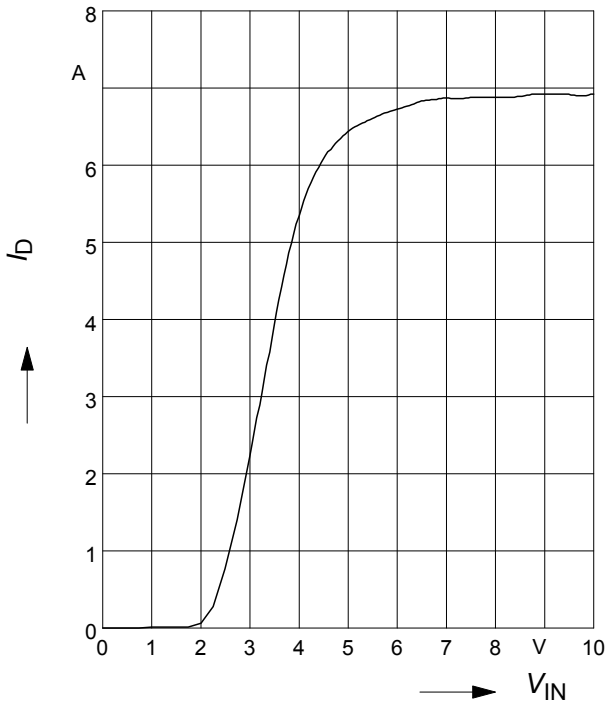
4 Typ. input threshold voltage

$V_{IN(th)} = f(T_j); I_D = 0.15 \text{ mA}; V_{DS} = 12V$



5 Typ. transfer characteristics

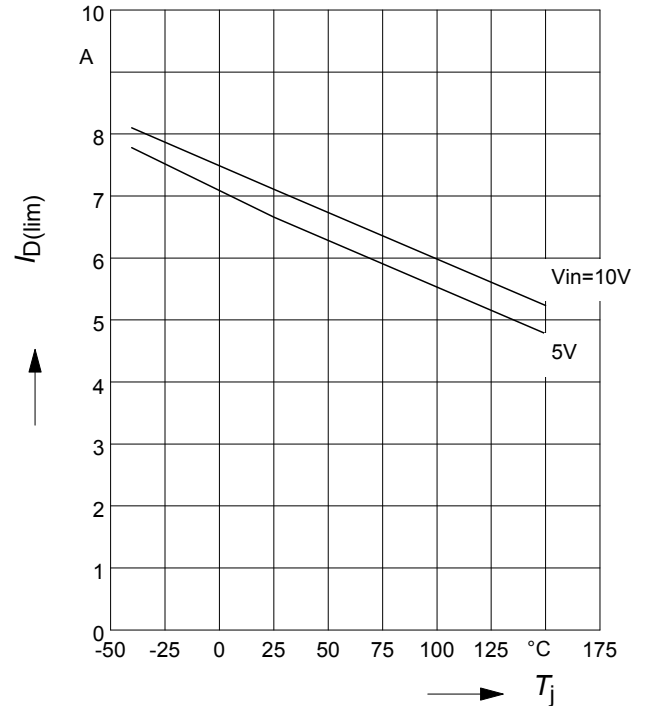
$I_D = f(V_{IN}); V_{DS} = 12V; T_{Jstart} = 25^\circ C$



6 Typ. short circuit current

$I_{D(lim)} = f(T_j); V_{DS} = 12V$

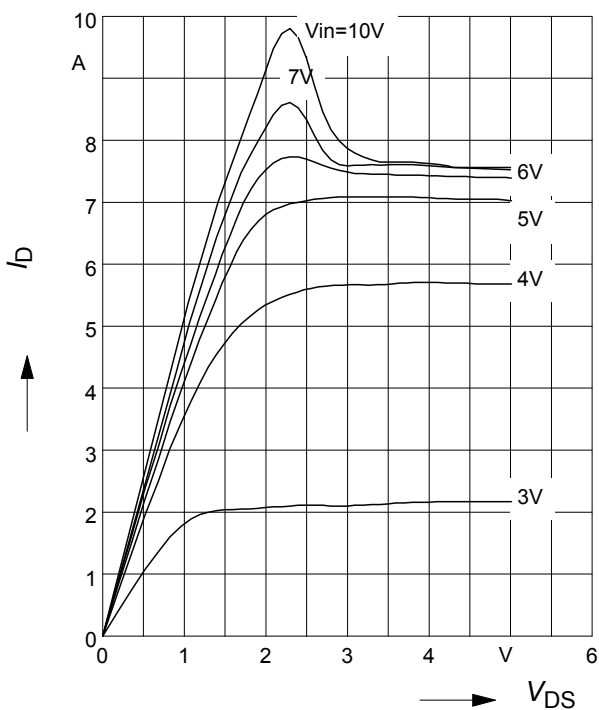
Parameter: V_{IN}



7 Typ. output characteristics

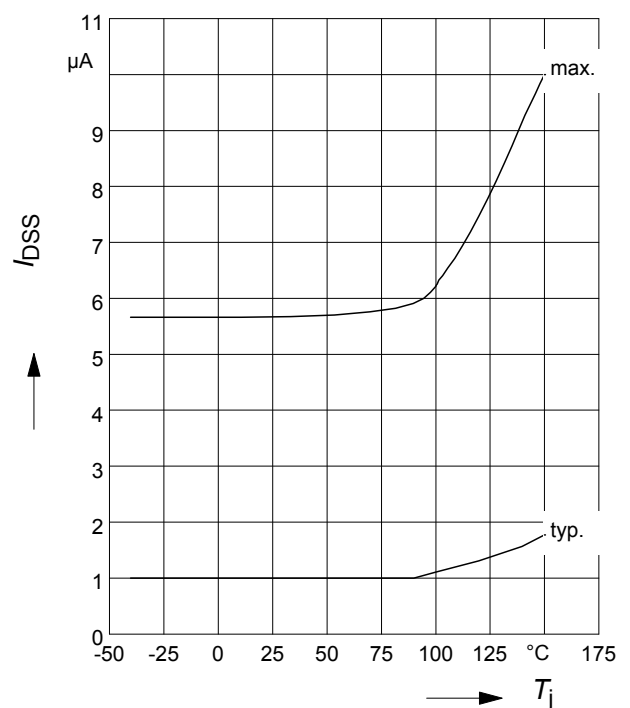
$I_D = f(V_{DS}); T_{Jstart} = 25^\circ C$

Parameter: V_{IN}



8 Typ. off-state drain current

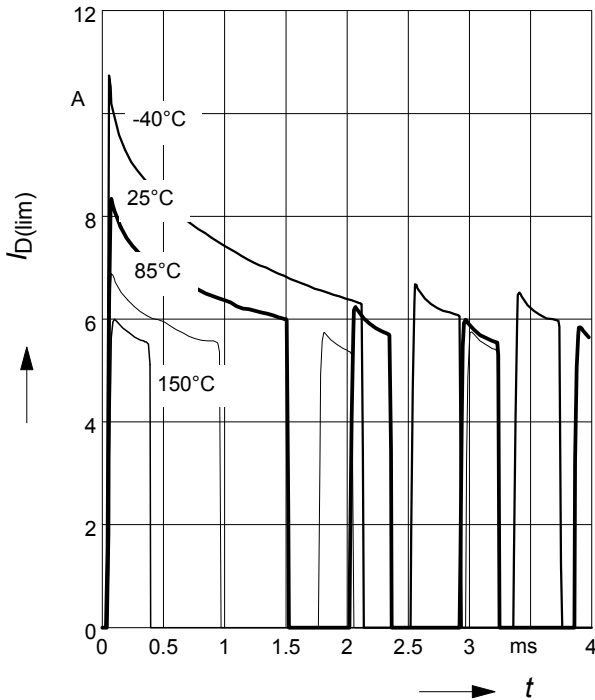
$I_{DSS} = f(T_j)$



9 Typ. overload current

$I_{D(lim)} = f(t)$, $V_{bb}=12\text{ V}$, no heatsink

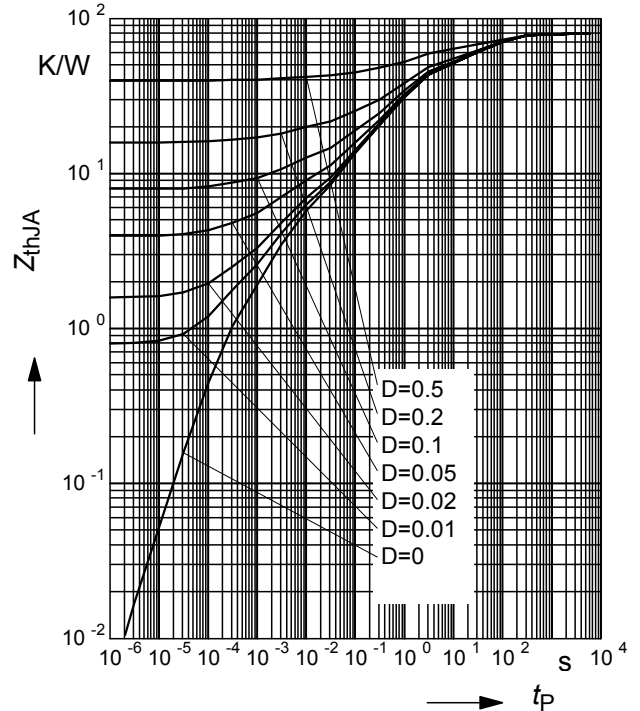
Parameter: T_{jstart}



10 Typ. transient thermal impedance

$Z_{thJA}=f(t_p)$ @ 6 cm² cooling area

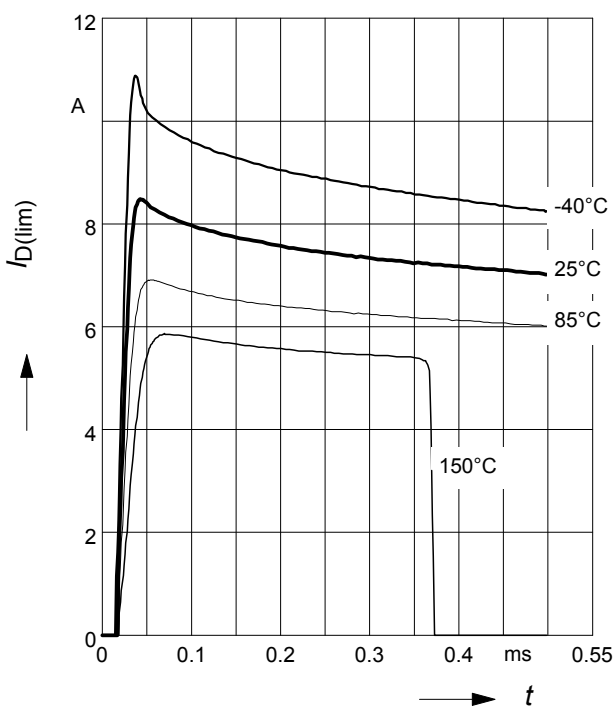
Parameter: $D=t_p/T$; one channel on



11 Determination of $I_{D(lim)}$

$I_{D(lim)} = f(t)$; $t_m = 200\mu\text{s}$

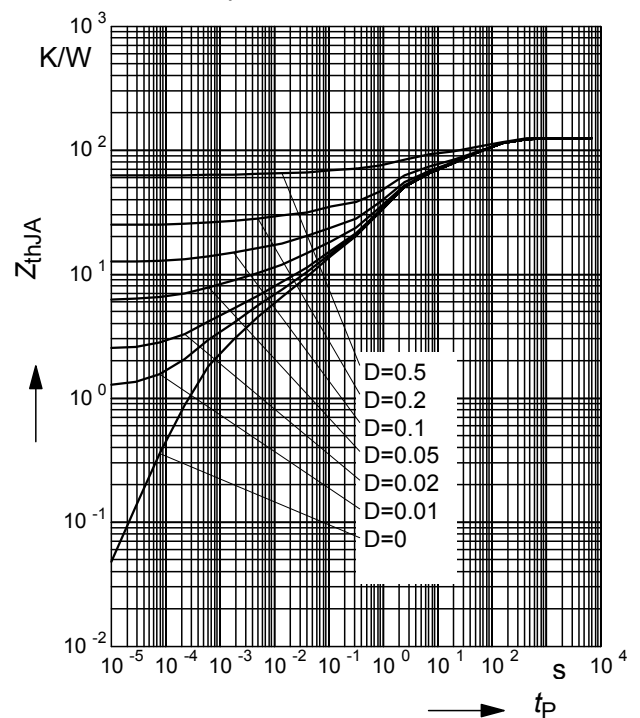
Parameter: T_{jstart}

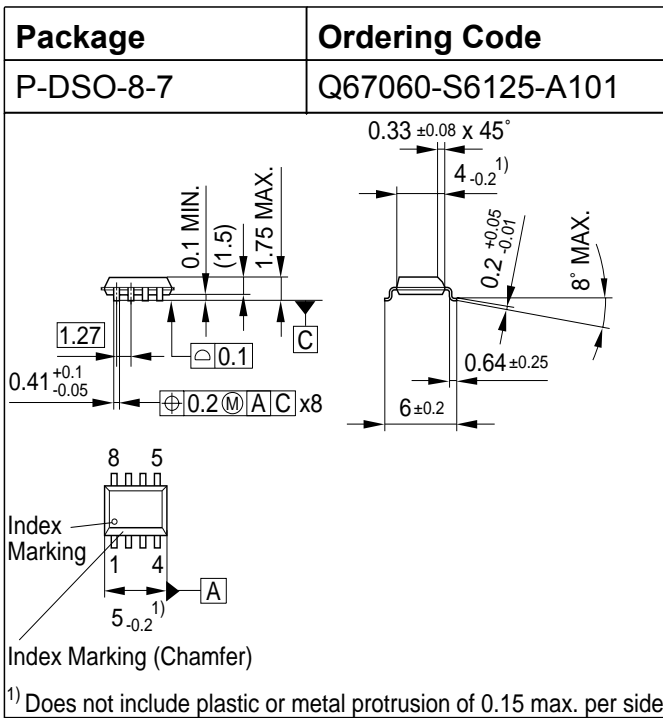


12 Typ. transient thermal impedance

$Z_{thJA}=f(t_p)$ @ 6 cm² cooling area

Parameter: $D=t_p/T$; both channels on





Revision History : 2004-03-05
 Previous version : 2003-04-22

Page	Subjects (major changes since last revision)
3, 6	Footnote 2 extended to $V_{in} < 0V$, E_{tot} and ΔT_{jT}
3, 4	Footnote 5 implemented to P_{tot} and $I_{D(nom)}$
3	ESD test condition changed from MIL STD 883D, methode 3015.7 and EOS/ESD assn. standard S5.1-1993 to Jedec Norm EIA/JESD22-A114-B, Section 4
3	Humidity category classification changed from DIN 40040 value E to J-STD-20-B value MSL1
3	climatic category changed from DIN IEC 68-1 to DIN EN 60068-1
4	$V_{IN(th)}$ test conditions from $I_D = 0.15mA$ to $I_D = 0.3mA$

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